

FIG. 1

PRIOR ART

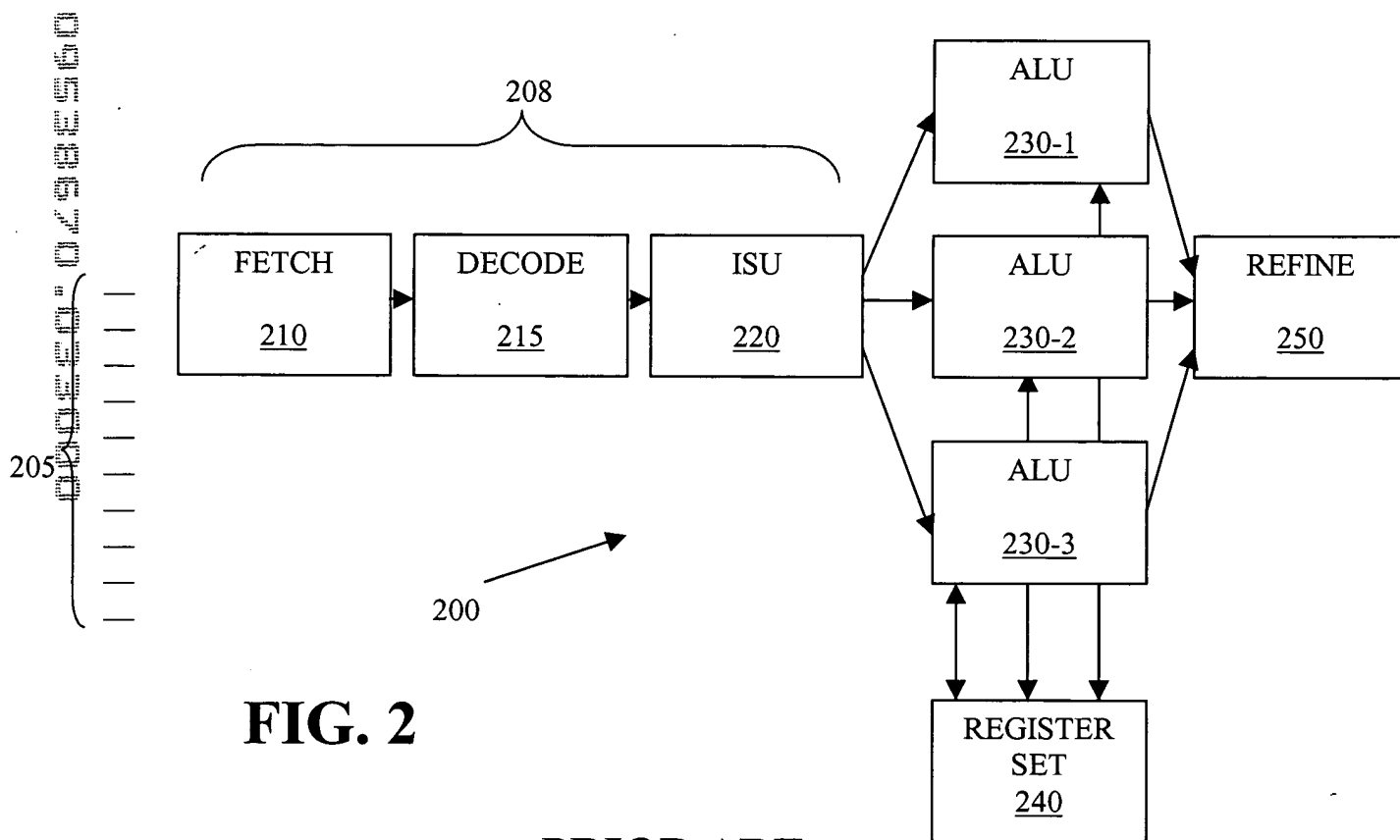


FIG. 2

PRIOR ART

310 { L3: ADD R0, R1, R2
L2: SUB R3, R4, R2
L1: OR R6, R1, R5

FIG. 3

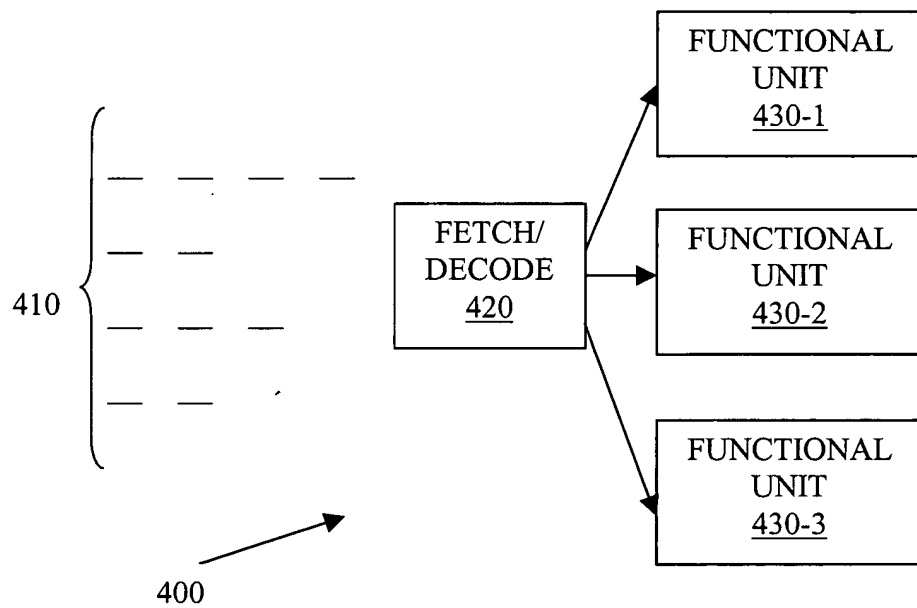


FIG. 4

PRIOR ART

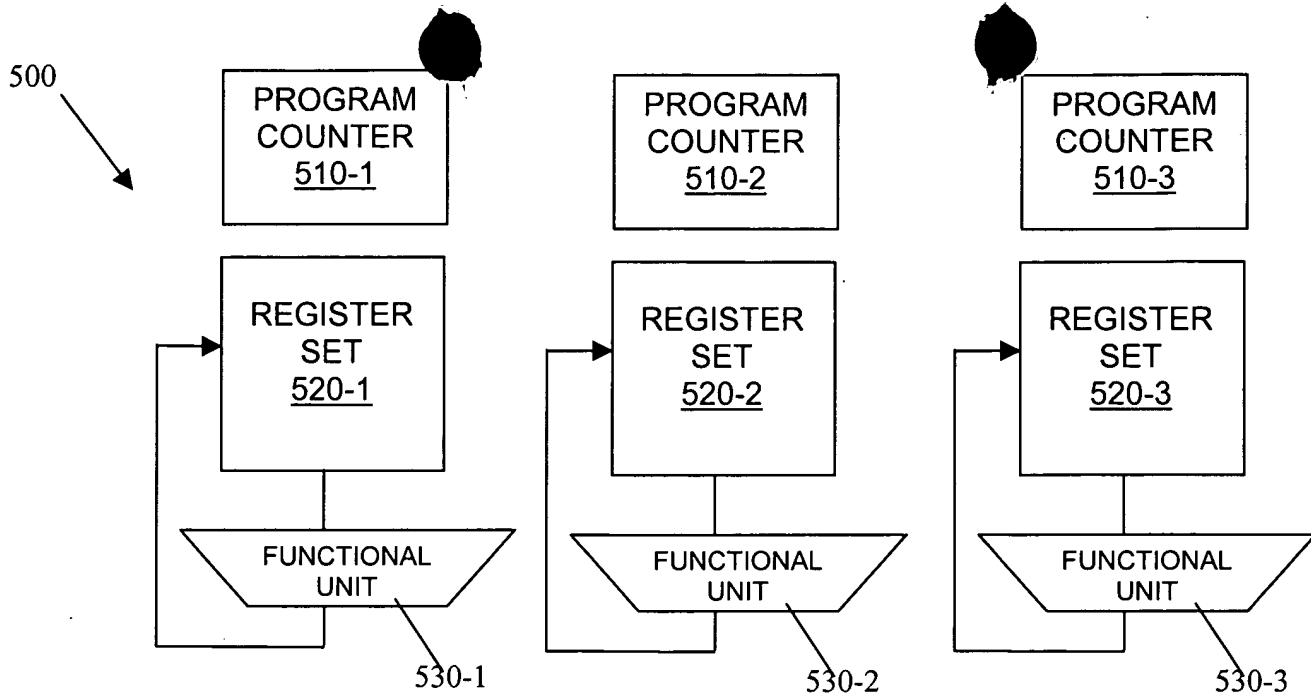


FIG. 5

PRIOR ART

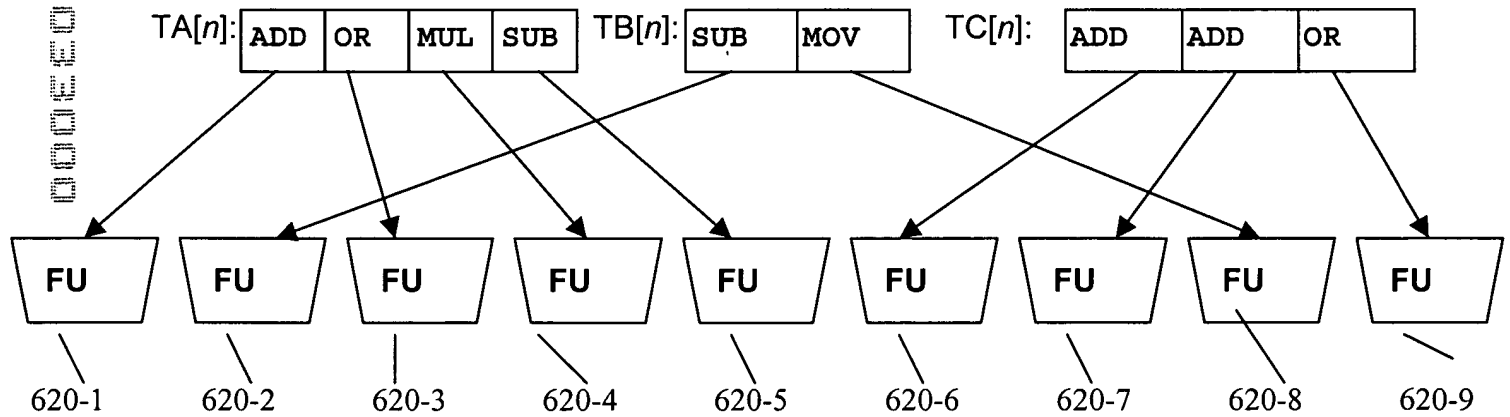


FIG. 6

700

FETCH GET A PACKET (UP TO K INSTRUCTIONS) FROM MEMORY <u>710</u>	DECODE DETERMINE FUs AND REGISTERS FOR UP TO K INSTRUCTIONS <u>720</u>	EXECUTE: PERFORM OPERATION AND PROCESS RESULT <u>730</u>
---	---	---

FIG. 7A

PRIOR ART

750

FETCH GET UP TO N PACKETS (UP TO K INSTRUCTIONS) FROM MEMORY <u>760</u>	DECODE DETERMINE FUs AND REGISTERS NEEDED FOR UP TO N*K INSTRUCTIONS <u>770</u>	ALLOCATE SELECT APPROPRIATE INSTRUCTIONS AND ASSIGN THEM TO FUs <u>780</u>	EXECUTE: PERFORM OPERATION AND PROCESS RESULT <u>790</u>
---	---	---	---

FIG. 7B

Figure 1 is a block diagram of a packet scheduling system 780. The system includes a Priority Encoder 810, an Input Crossbar Switch 820, and an Output Crossbar Switch 830. The Priority Encoder 810 receives inputs from three Priority LRU blocks and outputs Thread feedback signals (Packet assigned, Fetch next) and Busy signals. The Input Crossbar Switch 820 receives 3K inputs from N Register Files and outputs M outputs to the Output Crossbar Switch 830. The Output Crossbar Switch 830 outputs N*M or N*K writes.

FIG. 8